Amendments to the Specification

Please replace paragraph [0007] with the following amended paragraph:

[0007] Fig.2 shows a distribution plot of the threshold voltage of the memory cell 26 of Fig.1. The distribution plot of Fig.2 shows amount of the memory cells plotted against threshold voltage. For example, when a binary value "1" is to be stored in the memory cell 26, the memory cell 26 needs to be programmed such that the floating gate 18 will store more electrons and have a higher threshold voltage. For different memory cells 26, those which have "1" stored in them will not have the same threshold voltage, but will form a distribution like curve 28, more specifically they will have threshold voltages ranging from V11 to V12. On the contrary, when a binary value "0" is to be stored in the memory cell 26, the memory cell 26 needs to be erased such that that floating gate 18 will store fewer electrons and have a lower threshold voltage. For different memory cells 26, those which have "0" stored in them will not have the same threshold voltage, but will form a distribution like curve 30, more specifically they will have threshold voltages ranging from [[V21]] -V21 to -V22. Therefore, if a voltage between V11 and [[V21]] -V21 is inputted to every memory cell 26 of the flash memory 10, those with "0" stored in them will be turned on, and those with "1" will not be turned on. The binary data can be read according to the turn-on status through an external circuit, such as a sensing amplifier. Please note, the curves 28, 30 of the threshold voltage distribution are determined by the amount of electrical

charge on the floating gate 18, which means the curves 28 and 30 show the positive threshold voltage distribution as well as the negative threshold voltage distribution.

Please replace paragraph [0023] with the following amended paragraph:

[0023] Please refer to Fig.2, Fig.5, and Fig.6. Fig.6 shows a voltage level diagram of the bit line BL shown in Fig.3. First, a voltage is passed through the word line WL to the first electrode 60 to turn on the control unit 48. Therefore, the bit line BL will be electrically connected to the node A through the channel 65. If "1" is stored in the storage unit 46, the storage unit 46 will have a relatively high threshold voltage (between V11 and V12). Meanwhile, a smaller value of the memory cell capacitance Ccell will be produced due to fewer parasitic capacitors between the storage unit 46 and the control unit 48. When the word line WL inputs a voltage to the first electrode 60 of the control unit 48 in order to turn on the control unit 48, the bit line BL will be electrically connected to the memory cell capacitance Ccell through the channel 65 and the third electrode 64. At this moment, the remaining charges within the bit line BL and the memory cell capacitance Ccell will ~~redistributed~~ redistribute between the bit line BL and the memory cell capacitance Ccell. Therefore, if the original voltage level of the bit line BL is V1, then, starting from a time T0 when the bit line BL is electrically connected to the memory cell capacitance Ccell, the voltage level of the bit line BL will drop, and will reach a new voltage level V2, which is the same as that of the memory cell capacitance Ccell at a time T1. Similarly, if "0" is stored in the storage unit 46, the storage unit 46 will have a relatively low threshold

voltage (between [[V21]] -V21 and [[V22]] -V22). A larger value of the memory cell capacitance Ccell will be produced due to more parasitic capacitors between the storage unit 46 and the control unit 48. When the word line WL inputs a voltage to the first electrode 60 of the control unit 48 in order to turn on the control unit 48, the bit line BL will be electrically connected to the memory cell capacitance Ccell through the channel 65 and the third electrode 64. At this moment, the remaining charges within the bit line BL and the memory cell capacitance Ccell will redistribute between the bit line BL and the memory cell capacitance Ccell. Therefore, if the original voltage level of the bit line BL is V1, then, starting from the time T0 when the bit line BL is electrically connected to the memory cell capacitance Ccell, the voltage level of the bit line BL will drop, and will reach a new voltage level V3, which is the same as that of the memory cell capacitance Ccell at a time T2. By the mechanism described above, according to the different data stored in the storage unit 46, the bit line BL will be electrically connected to the memory cell capacitance Ccell and produce different levels of potential variation. By measuring this potential variation the correspondent binary value "0" or "1" can be determined.

Please replace paragraph [0025] with the following amended paragraph:

[0025] In summary, first the data is stored in the memory cell 42 in a non-volatile fashion through the amount of electrical charge stored in the floating gate 52, then the data is read from the storage unit 46 and is represented by the voltage level in the correspondent parasitic capacitors, i.e. the data is stored in a volatile fashion. Through the

mechanism described above, the non-volatile dynamic random access memory 40 will be able to access the stored volatile data rapidly like a conventional DRAM through the status of the voltage level at the node A, i.e. through the amount of the electrical charge stored in the memory cell capacitance Ccell. For example, when writing the data, a voltage is first inputted from the word line WL to turn on the control unit 48. Then, according to the data being "1" or "0" the second predetermined voltage (Vcc volts) or the third predetermined voltage (0 volts) will be inputted through the bit line BL, and the voltage level at the node A will approach the second predetermined voltage or the third predetermined voltage through the charging and discharging processes of the memory cell capacitance Ccell. When reading the data, a voltage is first inputted from the word line WL to turn on the control unit 48. Then a first predetermined voltage (for example 1/2 Vcc) will be inputted from the bit line BL. If "1" is stored in the memory cell 42, meaning the voltage level at node A is the second predetermined voltage (Vcc volts), the first predetermined voltage will discharge the memory cell capacitance Ccell and lower the voltage level at the node A. If "0" is stored in the memory cell 42, meaning the voltage level at node A is the third predetermined voltage (0 volts), the first predetermined voltage will charge up the memory cell capacitance Ccell and raise the voltage level at the node A. Therefore, the stored data can be determined by detecting and judging the variation of the voltage level at the node A.

Please replace paragraph [0026] with the following amended paragraph:

[0026] According to above-mentioned description, the

non-volatile dynamic random access memory 40 ~~is to input~~ inputs a higher voltage into the control gate 50 in order to eliminate the influence of the electrical charges stored on the floating gate 52 to the threshold voltage forming the channel 58. So no matter how much electrical charge is stored on the floating gate 52, a channel 58 in the substrate 44 will be formed and electrically connected to the control unit 48[[, i.e]]. [[the]] The memory cell capacitance Ccell, composed of parasitic capacitors of each memory cell 42, will approach a certain identical value and possess the same characteristics. At this moment, the data stored in each memory cell 42 will be transferred to a correspondent voltage level and the voltage level will start to charge or discharge the memory cell capacitance Ccell. Then the volatile data will be stored through the preservation of the voltage level in the memory cell capacitance Ccell. By doing so, the non-volatile data previously stored on the floating gate 52 of the storage unit 46 can be transferred into corresponding volatile data and stored through the preservation of the voltage level in the memory cell capacitance Ccell. Additionally, a refresh circuit (not shown in the figures) is needed to connect to the non-volatile dynamic random access memory 40. The refresh circuit is used to periodically refresh the data stored in the non-volatile dynamic random access memory 40 in order to prevent the potential loss or error of the volatile data due to reasons such as charge leakage of the memory cell capacitance Ccell.